ABSTRACT

A circuit layout structure for a chip is provided. The chip has a bonding pad area, a nearby device area, and a substrate. The circuit layout structure essentially comprises a plurality of circuit layers, a plurality of dielectric layers and a plurality of vias. The circuit layers are sequentially stacked over the substrate. Each dielectric layer is sandwiched between a pair of adjacent circuit layers. The vias pass through the dielectric layers and electrically connect various circuit layers. The farthest circuit layer away from the substrate has pluralities of bonding pads within the bonding pad area. The bonding pads near the device area overstrides at least one non-signal circuit layer through the furthest circuit layer away from the substrate and electrically connects to a circuit layer nearer the substrate with vias. The circuit layout structure can avoid a direct conflict of signals between the power/ground circuits and the signal circuits.